

Notice of References Cited	Application/Control No. 10/077,778	Applicant(s)/Patent Under Reexamination HIGUCHI ET AL.	
	Examiner Brian R. Peugh	Art Unit 2187	Page 1 of 2

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	J	US-			
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	L	US-			
	M	US-			

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	V	Ishibashi et al., "A 1.-V Adjustable I/O Interface for Low Voltage Fast SRAM's", © 1992 IEEE, p. 674-677.
	W	Aoki, et al. "A 60-ns 16-Mbit CMOS DRAM with a Transposed DATA-Line Structure", © 1988 IEEE, p. 1113-1119.
	X	Smith, "Intel's FLEXlogic FPGA Architecture" © 1993 IEEE, p. 378-384.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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